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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,197	06/13/2001	Michio Komoda	027260-468	4052

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EXAMINER	
FERRIS III, FRED O	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/879,197	KOMODA ET AL.
	Examiner	**Art Unit**
	Fred Ferris	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/01*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. *Claims 1-5 have been presented for examination based on applicant's disclosure filed on 13 June 2001. Claims 1-5 have been rejected by the examiner.*

Priority

2. *Applicant's claim for priority based Japanese application 2000-314251 filed on 13 October 2000 is acknowledged. Receipt is acknowledged of the priority papers submitted under 35 U.S.C. 119(a)-(d), which have been placed of record in the file.*

Drawings

3. *Drawings submitted on 13 June 2001 have been reviewed and are approved by the examiner.*

Claim Objections

4. *Claim 1 is objected to because of the following informalities: The phrase on page 25, line 10 contains a typographical error and reads, "a <u>fist</u> region" but should read "a <u>first</u> region" as disclosed throughout applicant's specification. Appropriate correction is required.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over "CMOS Gate Delay Models for General RLC Loading", R. Arunachalam et al, Proceedings International Conference on Computer Design, ICCD 97', IEEE 1997, in view of "A Comprehensive Submicrometer MOST Delay Model and its Application to CMOS Buffers", P. Cocchini et al, IEEE Journal of Solid-State Circuits, Vol. 32, No. 8, August 1997.

Independent claim 1 is drawn to the following elements.

<u>Delay time estimation for logic circuit by</u>:
Modeling MOS transistor by resistive element having
  Fixed resistance
  Time varying power source voltage
Segmenting modeled MOS transistor characteristic into regions
  First region where current increases as gate potential varies
  Second (saturation) region where current decreases for constant gate potential
  Third (linearity) region where current decreases for constant gate potential

<u>Regarding independent claim 1</u>: Arunachalam discloses a model for delay time estimation of a logic circuit in terms of a <u>time varying voltage source</u> in series with <u>a</u>

<u>constant (fixed) resistance</u> (Abstract, page 224, column 2, lines 6&7). Arunachalam teaches the elements of the claimed limitations of the present invention (claim 1) as follows:

<u>Delay time estimation for logic circuit</u>: Arunachalam discloses a model for delay time estimation of a logic circuit. (Pages 226-229, Section 3.3)

<u>Modeling MOS transistor by resistive element</u>: Arunachalam teaches a model for a logic circuit (gate level) that includes a resistive element (fixed resistance). (Abstract, Sections 2&3, pages 226-229, Section 3.3, Figs. 1-5), (See below: <u>Cocchini</u> teaches a <u>transistor level</u> model)

<u>Fixed resistance</u>: Arunachalam teaches a model for delay time estimation in a logic circuit that includes a <u>fixed (constant) resistance</u>. (Abstract, page 225, column 1, lines 10&11, page 225, Section 3.0, page 226, Section 3.1, page 224, column 2, lines 6&7, Section 4, Figs. 4-10)

<u>Time varying power source voltage</u>: Arunachalam teaches a model for delay time estimation in a logic circuit that includes a <u>time varying voltage source</u> model. (Abstract, page 225, column 1, lines 10&11, page 226, Section 3.2, page 224, column 2, lines 6&7, Section 4, Figs. 4-10)

Arunachalam does not explicitly teach <u>segmenting a transistor model into regions</u> of device operation.

Cocchini discloses a <u>transistor level model</u> for delay time estimation of a logic circuit that includes <u>segmenting the transistor model</u> into <u>regions of device operation</u>

including off, saturation, and linearity regions. Cocchini teaches the elements of the claimed limitations of the present invention (claim 1) as follows:

<u>*Segmenting modeled MOS transistor characteristic into regions*</u>*: Cocchini discloses segmenting the* <u>*transistor model*</u> *into* <u>*regions of device operation*</u>*. (Figure 2, pages 1255-1257, Section III: MOST Delay Model) Cocchini actually teaches beyond the requirements of the claimed limitations of the present invention in that there are five regions but includes the claimed elements of the first, second and third region as a subset. (See below)*

<u>*First region where current increases as gate potential varies*</u>*: Cocchini discloses a region where current is increasing as the gate potential varies. For example, in Region 0 of Cocchini, the current is increasing (charging) as the input voltage (and hence the output voltage (Vo)) increases (i.e. varies). (See: page 1255, column 1, paragraph 4, Section III MOST Delay Model, Equation 7)*

<u>*Second (saturation) region where current decreases for constant gate potential*</u>*: Regions 1 and 2 of Cocchini disclose saturation regions of the transistor model. In Region 2, for example, Cocchini discloses a* <u>*saturation region*</u> *where the charge is now decreasing (negligible) and Vi is now equal to Vdd (i.e. constant). (See: page 1256, column 1, last paragraph (Section C. Region 2))*

<u>*Third (linearity) region where current decreases for constant gate potential*</u>*: Regions 3 and 4 of Cocchini disclose linearity regions of the transistor model. In Region 4, for example, Cocchini discloses a* <u>*linearity region*</u> *where the charge is now*

decreasing (negligible) and input voltage is constant and equal to Vdd. (See: page 1257, column 1, 2nd paragraph (Section E. Region 4))

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Arunachalam relating to a modeling delay time of a logic circuit in terms of a time varying voltage source in series with a constant (fixed) resistance, with the teachings of Cocchini relating to a transistor level model for delay time estimation of a logic circuit that includes segmenting the transistor model into regions of device operation, to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many types of delay time estimation techniques available in the market place (see Dagenais Abstract, for example) and large amounts of money being spent in product development and improvement to solve problems arising from modeling logic circuit delays for increased signal speeds. (See: Cocchini and Arunachalam, Introductions) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Arunachalam with the teachings of Cocchini in order to reduce development time and cost.

Dependent claim 2 is further drawn to:
A circuit of a plurality of logic circuits including MOS transistors by;
Segmenting logic circuit last-stage MOS transistor characteristic into
- First region where current increases as gate potential varies
- Second (saturation) region where current decreases for constant gate potential
- Third (linearity) region where current decreases for constant gate potential

Regarding dependent claim 2: Dependent claim 2 merely requires that the elements of claim 1 relating to segmenting the logic circuit into regions be applied to a plurality of logic circuits comprised of MOS transistors to a final stage logic element. Arunachalam teaches delay time estimation modeling of gate and cell level (multiple logic circuits) logic circuits (i.e. a plurality or logic circuits (all stages)) as noted above. Cocchini discloses a transistor level model (MOS transistors) for delay time estimation of a logic circuit that includes segmenting the transistor model into regions of device operation (saturation, linearity, etc.) as noted above. Accordingly, these limitations are rendered obvious in view of the reasoning and prior art as previously cited above.

Dependent claim 3 is further drawn to:
(E) Powers source voltage = Rs (resistance model of power source) x (i) charge current of load model (t) + (v) charge voltage of load model (t).

Regarding dependent claim 3: The equation of claim 3 requires that the voltage (E) of the power source be equal to the resistance model (Rs) times the charge current (i) plus the charge voltage (v) of the load model for time ($\Delta t_{1,2}$) required to reach the power source voltage (boundary). (i.e. a time based representation of the fixed resistive element and power source voltage) Arunachalam teaches the resulting gate effects of a time-varying voltage source and a fixed resistive element for a wide range of effective capacitive load values represented as time duration slope ramps (curves) of gate voltage. (See Arunachalam pages 226-229, Section 3.1-4.0, Figs. 4-10, page 227, especially paragraphs 2-6) The examiner further notes that both the source and load models have been disclosed by applicants to be known prior art. (See: specification page 3, lines 6-27)

Dependent claim 5 is further drawn to:
Computer code program medium of claim 1 limitations

Regarding dependent claim 5: Dependent claim 5 merely claims the computer program medium for the program code to perform the method claimed in independent claim 1 and is therefor rejected using the same reasoning as cited above.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over "CMOS Gate Delay Models for General RLC Loading", R. Arunachalam et al, Proceedings International Conference on Computer Design, ICCD 97', IEEE 1997, in view of "A Comprehensive Submicrometer MOST Delay Model and its Application to CMOS Buffers", P. Cocchini et al, IEEE Journal of Solid-State Circuits, Vol. 32, No. 8, August 1997, and in further view of U.S. Patent 6,629,299 issued to Iwanishi.

Dependent claim 4 is further drawn to:
A delay library specifying model lines of Ids-Vds characteristic at given potential and slew rate for fixed delay

Arunachalam teaches the elements of independent claim 1 relating to a modeling delay time of a logic circuit in terms of a time varying voltage source in series with a constant (fixed) resistance as cited above. Cocchini teaches the elements of independent claim 1 relating to a transistor level model for delay time estimation of a logic circuit that includes segmenting the transistor model into regions of device operation as also cited above.

Arunachalam further does not explicitly teach a delay library for specifying delay parameters and model lines of characteristics (slew rates).

Regarding dependent claim 4: Iwanishi teaches the use of a delay library (CL2-L17-33, Figs. 1, 8)for storing and specifying parameters (CL3-L7-15, Figs. 1, 8) relating to the slew rates (Abstract, CL3-L7-15, Figs. 2-4) of signal waveforms (CL3-L16-31) of cell delay based on time intervals (CL3-L16-31) and load capacitance (Abstract, Summary, Figs. 1, 4, 8, 11, 12). Hence, a skilled artisan would have been motivated for the reasons previously cited above, to further modify the teachings of Arunachalam with the teachings Iwanishi to include the Ids-Vds characteristics in a delay library. The examiner further notes that the use of a "library" for storing CAD based parameters relating to circuit design is very well known in the art. Library features for storing circuit design parameters are included with any popular commercially available CAD design programs such as SPICE, ProEngineer, and AutoCAD.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,066,177 issued to Iwanishi teaches time delay estimation in logic circuits and a delay library.

U.S. Patent 6,606,587 issued to Nassif et al teaches time delay estimation in logic circuits.

U.S. Patent 6,099,576 issued to Jiang teaches time delay estimation in logic circuits.

"Efficent Gate Delay Modeling for Large Interconnect Loads", A.B. Kahng et al, IEEE 0-8186-7286-2/96, IEEE 1996 teaches time delay estimation in logic circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

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